Incremental ADC testing

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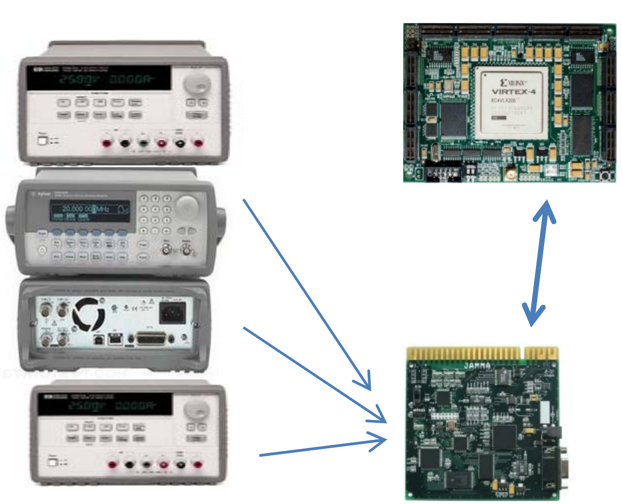
Measurement Setup

PC communication to ADC board takes place through FPGA board.

FPGA runs at 2 different frequencies. ADC interface part of the FPGA runs at the sampling frequency of the ADC (<4MHz) while the rest of it operates at 100MHz. Fast operation of part of FPGA for storing data and communication to PC is necessary for real-time data acquisition for the whole system. Internal data transfer between these two parts of the FPGA is achieved using shared memory FIFOs.

FPGA board



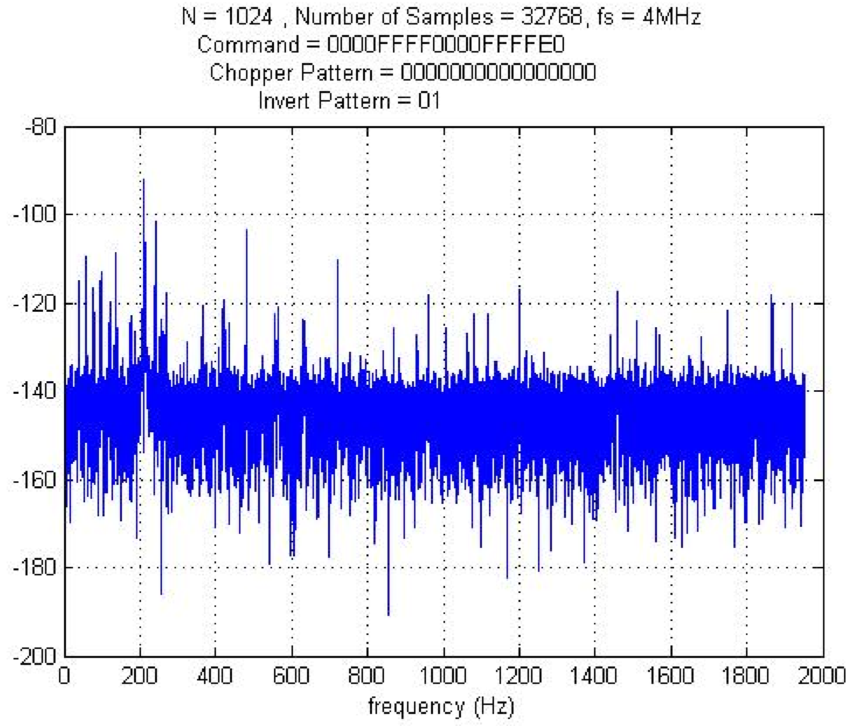
ADC board

My work can be divided into 3 parts: Matlab/Simulink modifications, doing measurement, modifying the ADC board

Noise-floor Tones

- Differential inputs were short circuited on the board.
- Agilent E3631A Triple Output Power Supply was used as a 4V digital supply and also a 1.65V common mode voltage reference.
- Keithley 2400 SourceMeter was used for 3.3V DAC voltage reference. By the time of this measurement it was assumed that Keithley has the lowest noise among the available sources.
- Comparing 5 different cases

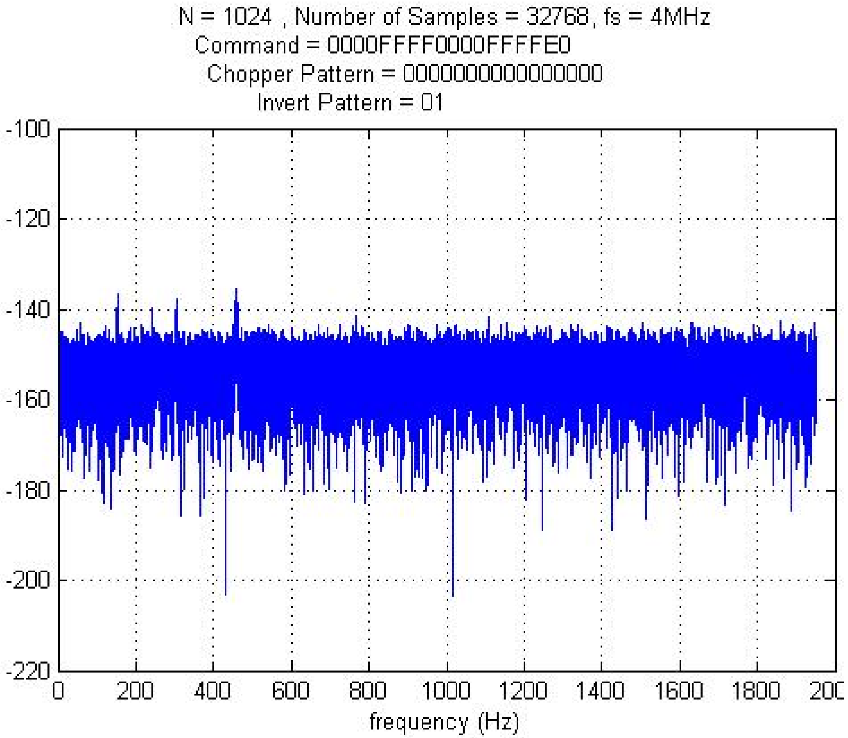
CASE 1:
inputs short circuit and VREFN to GND connection both were made using long wires (around 30cm).

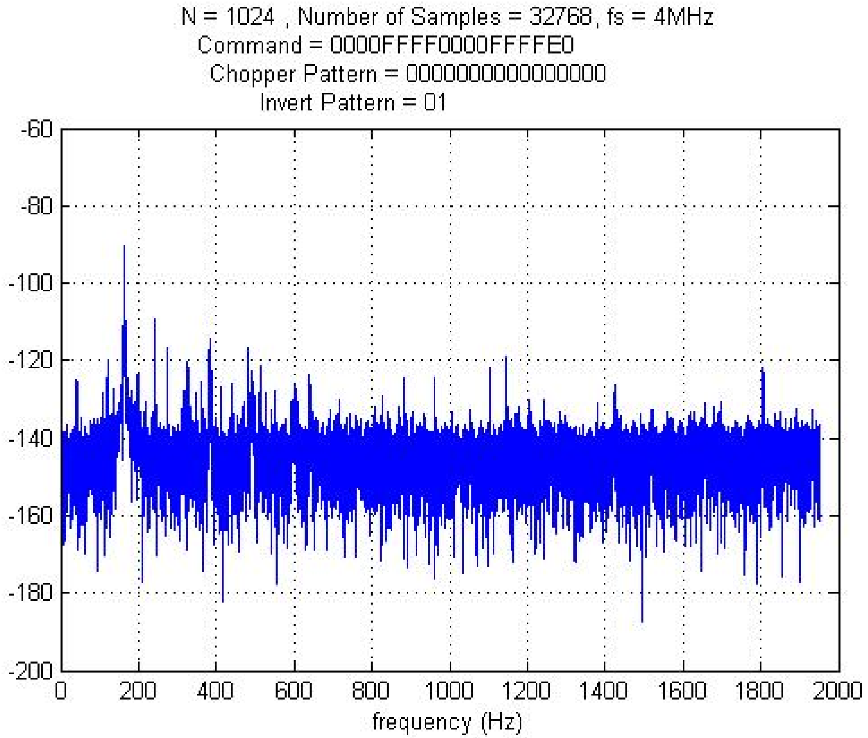


Noise-floor Tones

CASE 2:
inputs short circuit and VREFN to GND connection both were made using short wires (around 1cm) and jumpers.

CASE 3:
inputs short circuit was made using a long wire (around 30cm). VREFN to GND connection was made using a short wire (around 1cm) and jumpers.

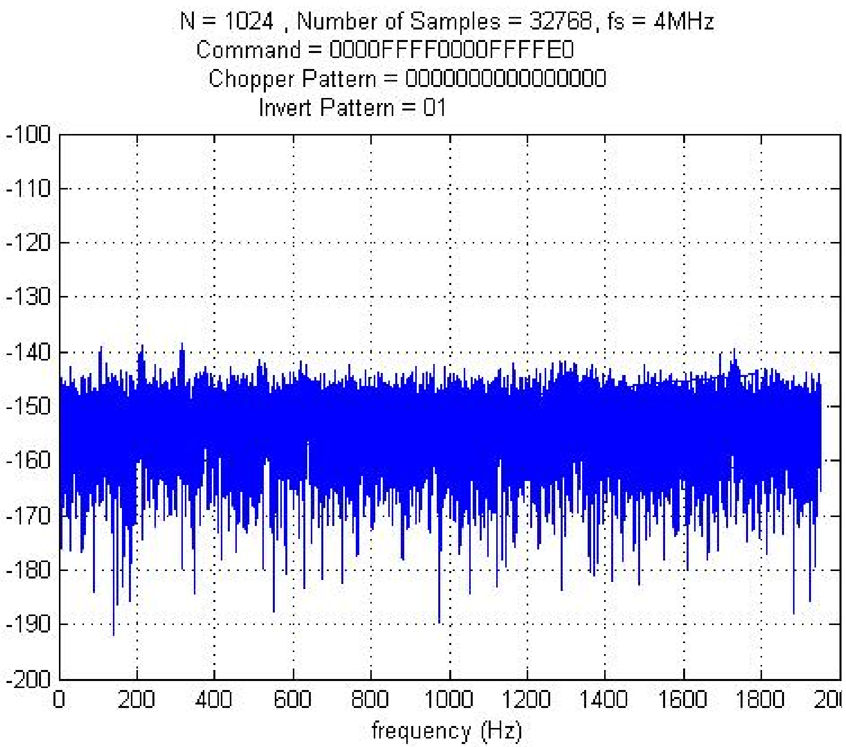




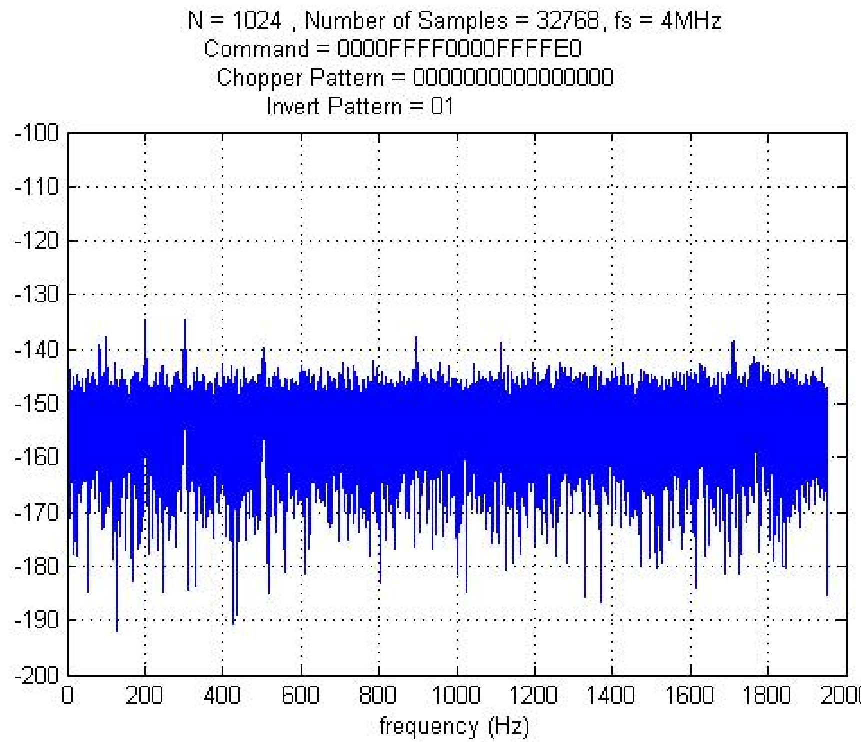
Noise-floor Tones

3 AA batteries which were used for analog supply were substituted with Agilent E3634A DC Power Supply.

CASE 4:
inputs short circuit and VREFN to GND connection both were made using short wires (around 1cm) and jumpers.



CASE 5:
inputs short circuit was made using a short wire (almost 1cm). VREFN to GND connection was made using a long wire (around 30cm).



Noise-floor Tones Conclusion

- Using long wires (hence bigger loops) for making connections were the source of all the tones.
- Using long wire (hence bigger loop) for short circuiting the inputs was the main source of most of the tones.
- Shielded twisted pair cable is best for the differential input signals.

Note:

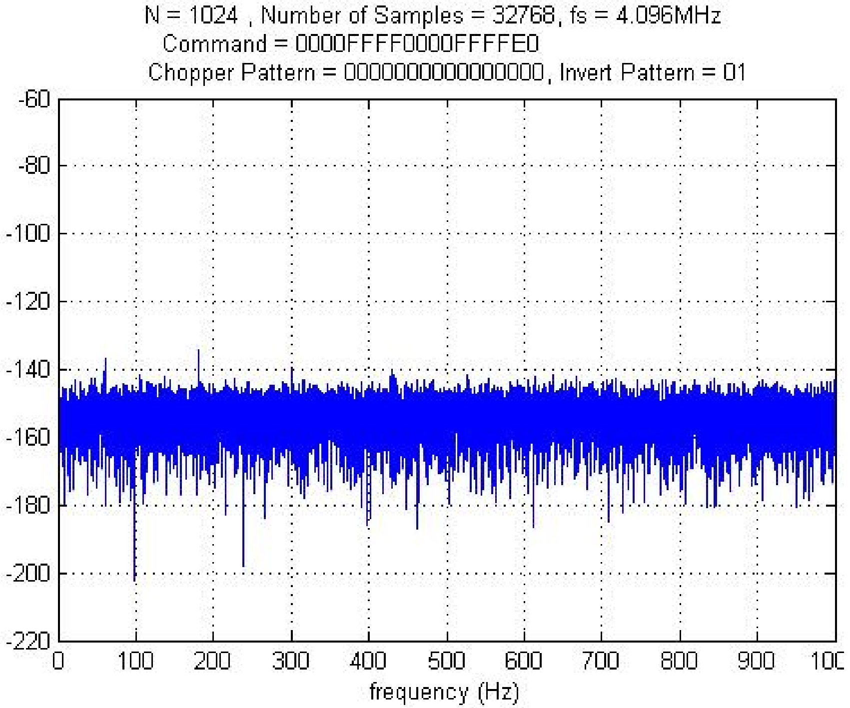
Making ground loops can generate more noise and big tones. The shielding should never be grounded at both ends.

Shielded Twisted Pair (Sine wave input)

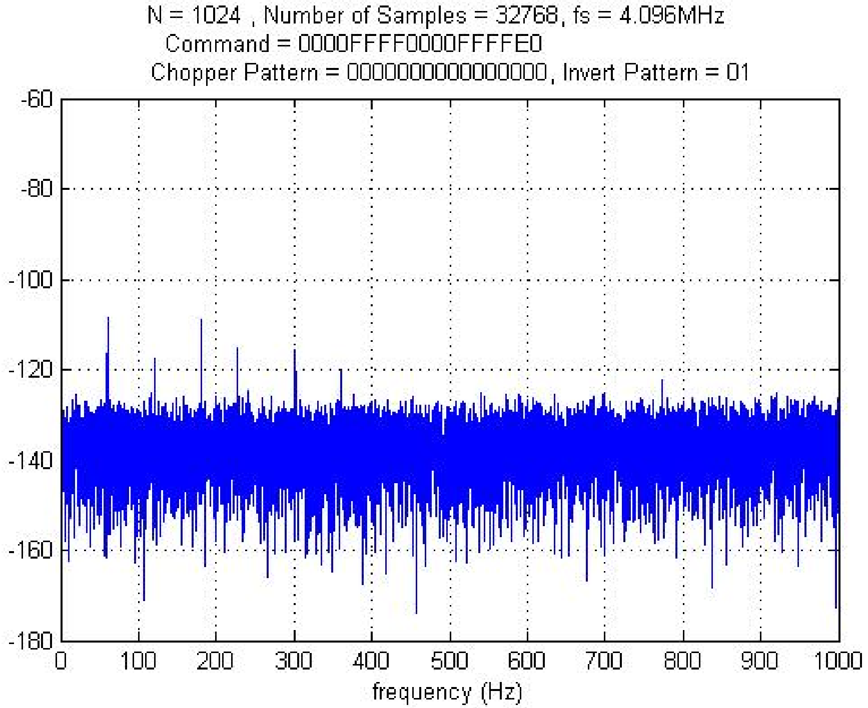
HP E3633A was used for 3.3V DAC voltage reference. Agilent E3631A was used for common mode voltage reference. DAC reference voltage was provided by a shielded twisted pair.

The inputs are short circuited right at the DC common mode voltage source.

Shielded twisted pair (noise-floor @ -145dB)



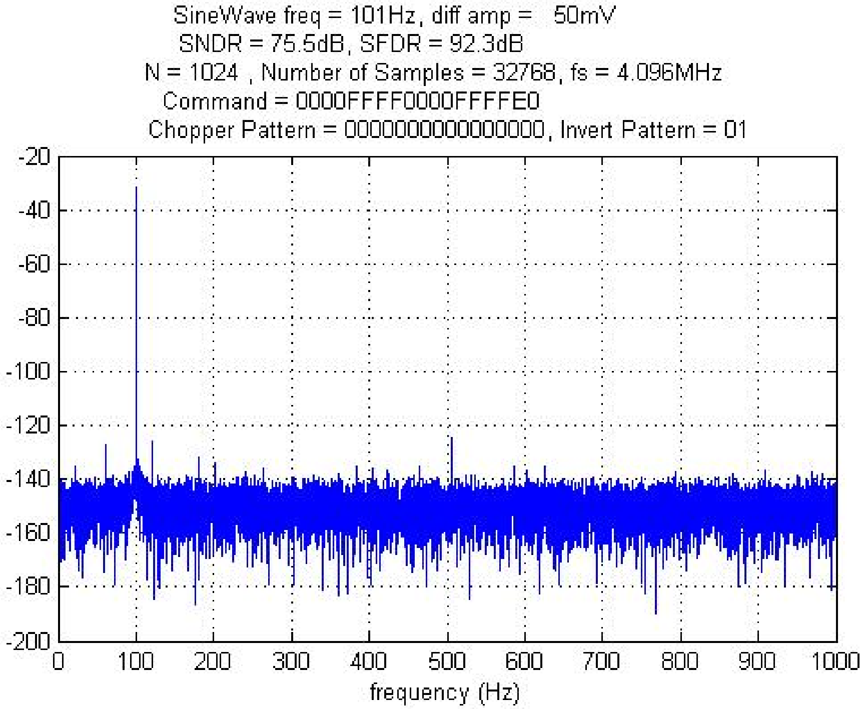
Twisted coax (noise-floor @ -130dB)



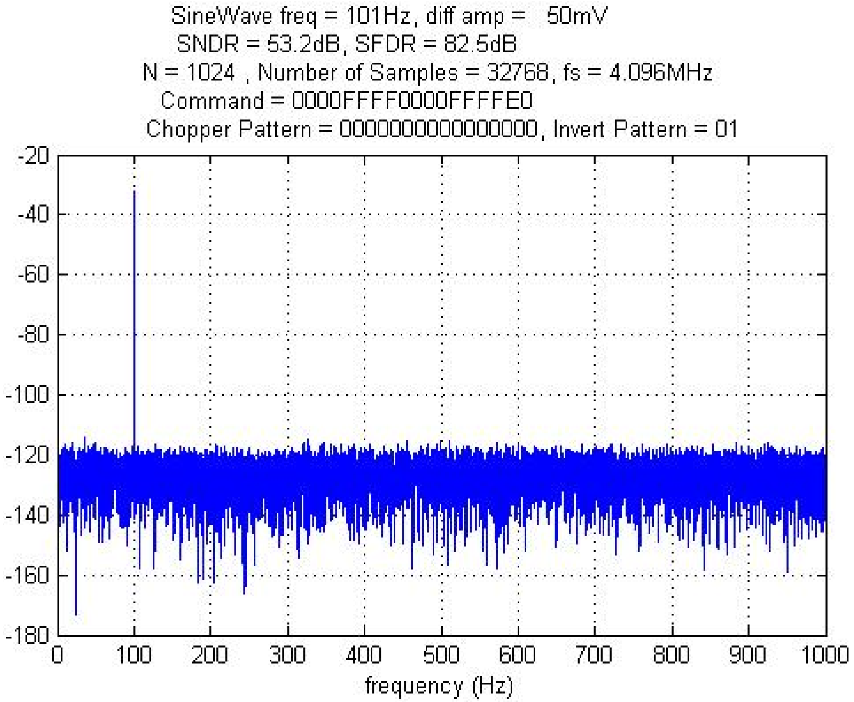
Shielded Twisted Pair (Sine wave input)

Shielded twisted pair shows the best performance among other connections. Although the connection for twisted coax was not as good as shielded twisted pair due to use of extra adaptors.

Shielded twisted pair (noise-floor @ -140dB)



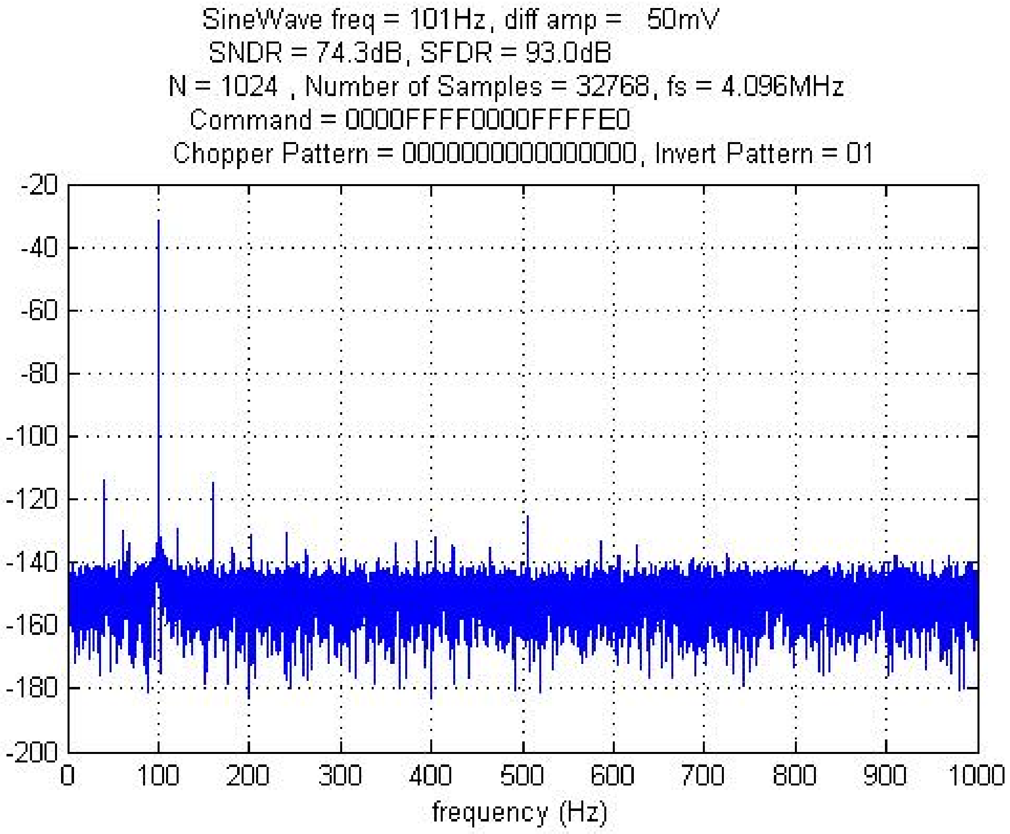
Twisted coax (noise-floor @ -120dB)



Comparing DC Sources (Sine wave input)

Shielded twisted pair was used for both differential input and DAC voltage reference connections in all cases.

Input sine wave was provided by Stanford Research System waveform generator.



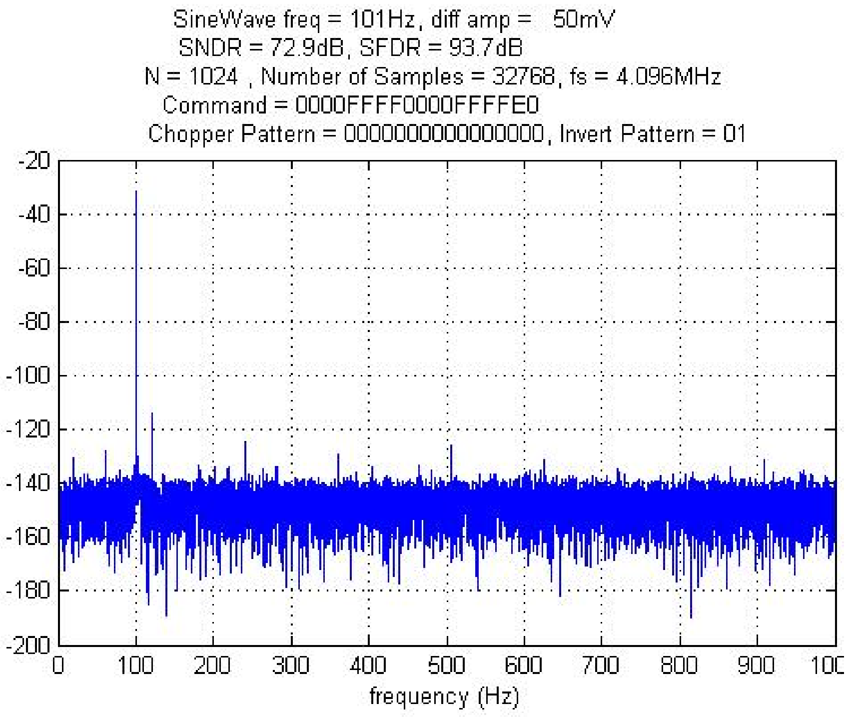
Using Keithley device as the 3.3V DAC voltage reference.

Two big 60Hz input side tones are clearly visible.

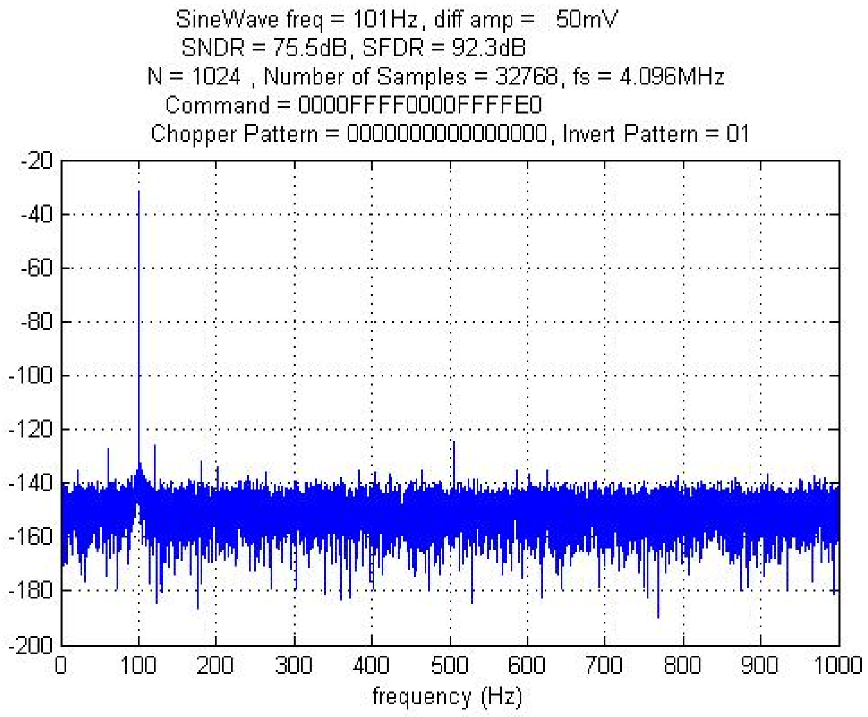
Comparing DC Sources (Sine wave input)

Agilent E3631A is a bit noisier than HP E3633A, while Keithley is noisier than both of them.

using Agilent E3631A for DAC reference

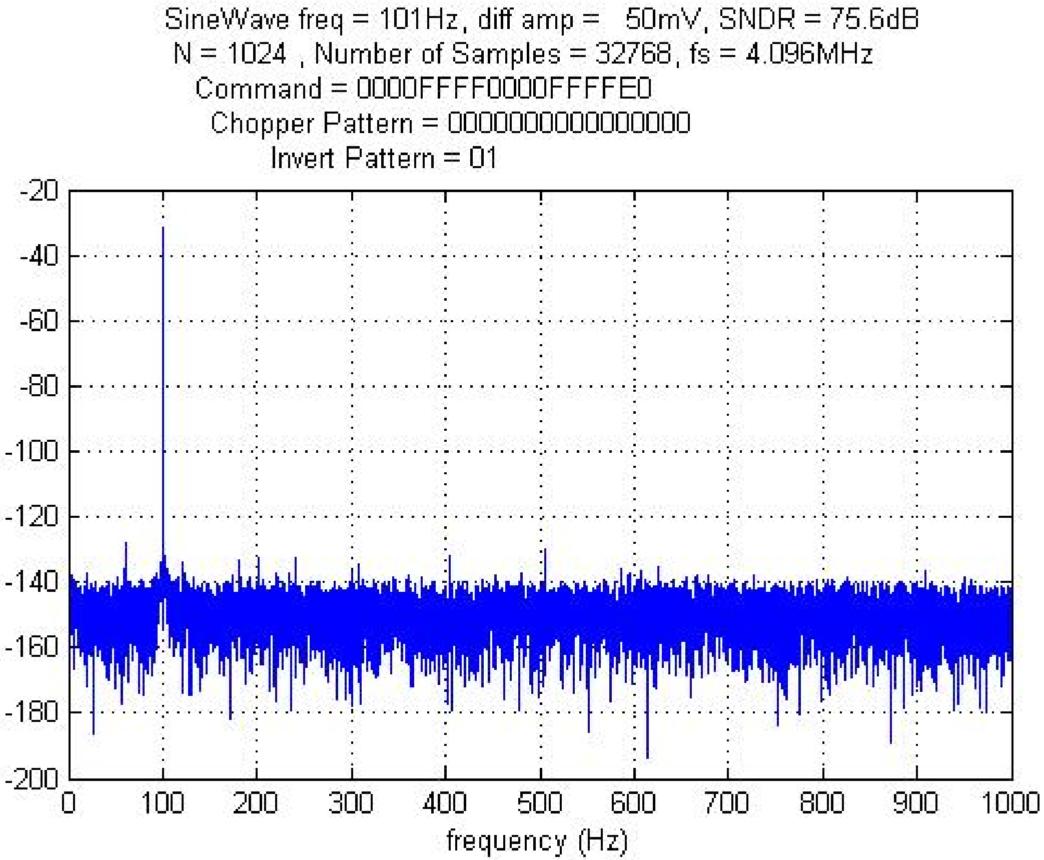


using HP E3633A for DAC reference



Comparing DC Sources (Sine wave input)

Using batteries for all the voltage references and supplies (bypassing the board regulators) SNDR is improved to 75.6dB and SFDR improved to around 98dB.



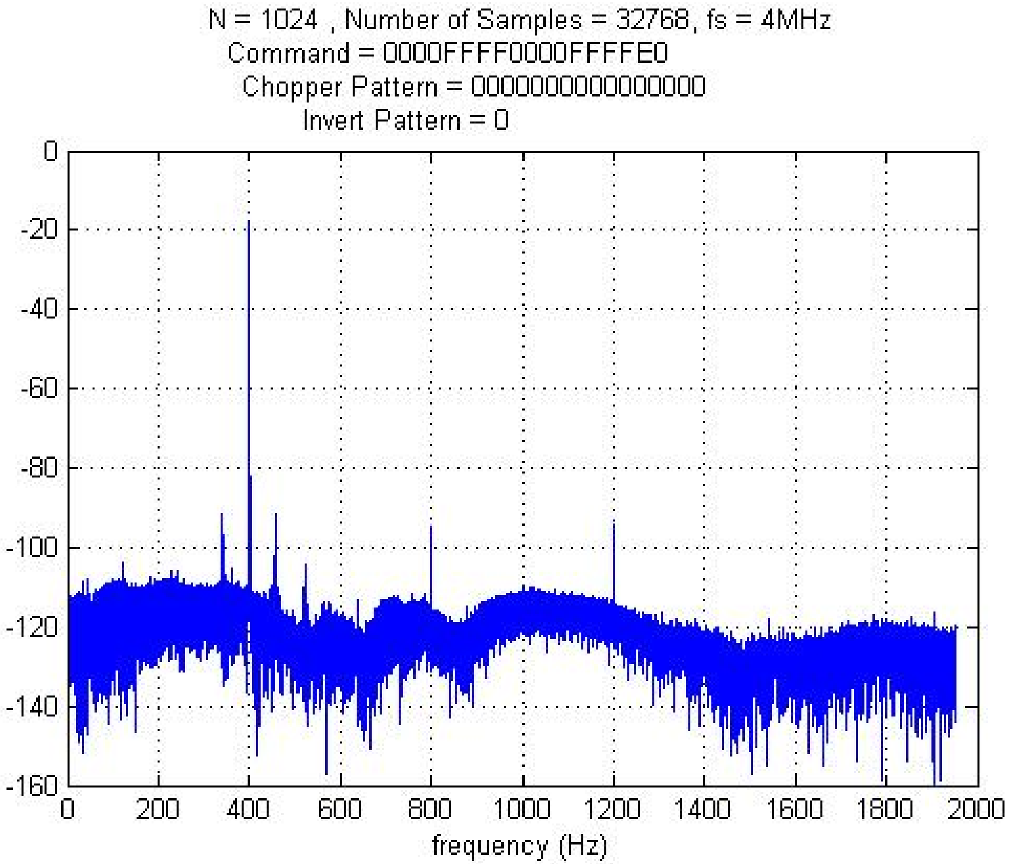
60Hz tones are still visible in the noise floor as the input tone is generated by Stanford Research device.

Note:

For peak SFDR measurements it is likely that higher order harmonics dominate the 3rd order harmonic.

Sine wave Measurements

An example which combines several points. Due to a factor of 2 mistake in single-ended and differential input amplitude calculation the ADC was overloaded which raised the noise-floor considerably.

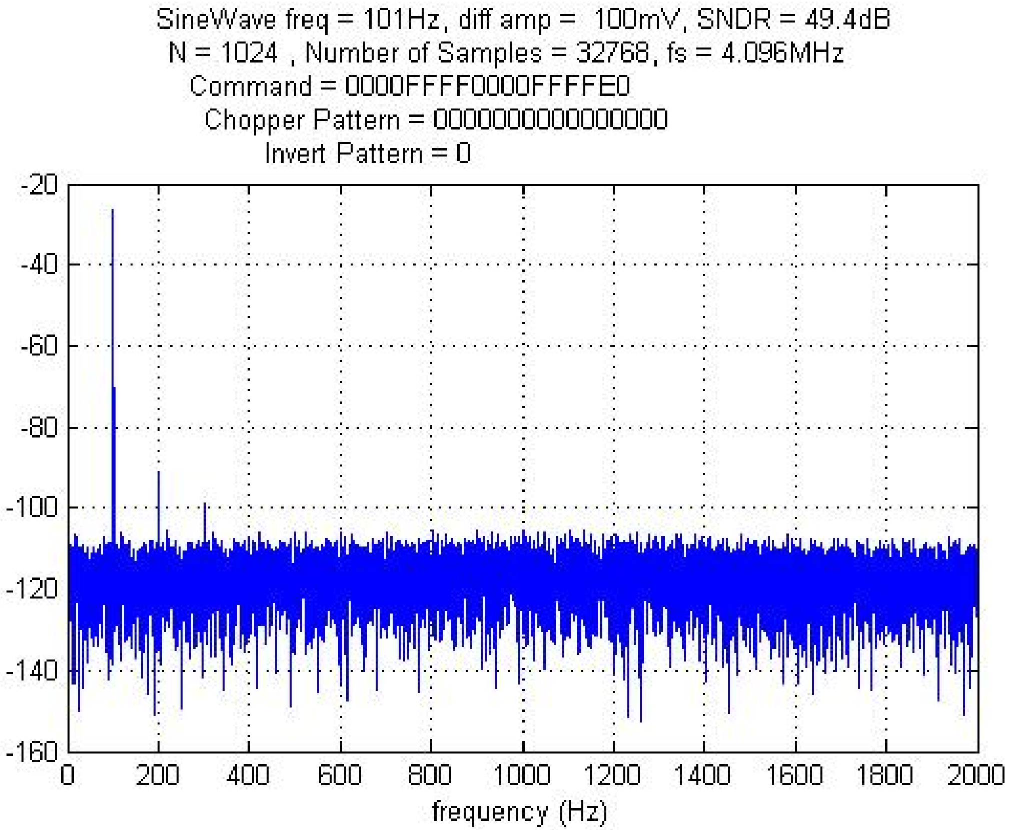


Shape of the noise floor was due to “hann” windowing.

Keithley effect, two 60Hz side tones, is clearly visible next to the signal tone.

Windowing

An almost similar situation where instead “nuttallwin” function was used for windowing. Shape of the noise floor is more regular.

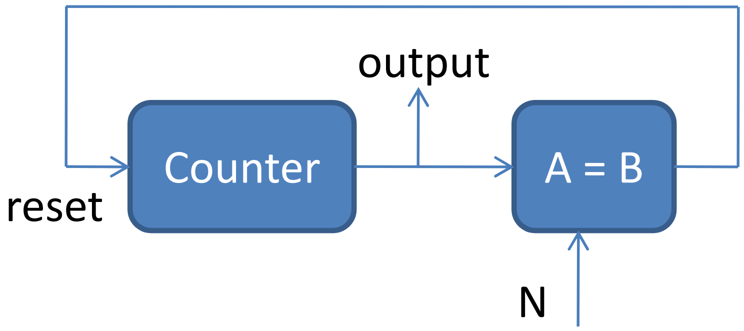


When input tone and sampling clock are not synchronized “nuttallwin” needs less number of FFT bins than “hann” to capture the same amount of energy of input tone.

Matlab/Simulink

- Make sure to “latch” FPGA before reading it or you will struggle with getting “0”s !

- When using counters make sure that reset cycle doesn’t make a problem. For example, assuming a 4 bit counter and N = 4, during reset cycle the output will be N+1 and during the next cycle it will be zero.



- When using “concat” block for concatenating bits double check your codes to ensure that MSB and LSB bits are taken into account in correct order.

Modifying the board

- OrCAD can be tricky when doing the layout of the PCB ! It takes time to get comfortable doing layout with it.