

A 24/77GHz Dual-Band BiCMOS Frequency Synthesizer

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Abstract — The design of a millimeter-wave dual-band phase-locked frequency synthesizer in a 0.18 μm SiGe BiCMOS technology is presented. All circuits except the voltage controlled oscillators (VCOs) are shared between the two bands. A W-band divide-by-3 frequency divider is used inside the loop after the VCOs to simplify division-ratio reconfiguration. The 0.9mm² synthesizer chip exhibits a locking range of 23.8-26.95/75.67-78.5GHz with a low power consumption of 50-75mW from a 2.5V supply. The closed-loop phase noise at 1MHz offset from the carrier is less than -100dBc/Hz in both bands. The proposed frequency synthesizer is suitable for integration in direct-conversion transceivers for K/W-band automotive radars and heterodyne receivers for 94GHz imaging applications.

Index Terms — BiCMOS integrated circuits, frequency synthesizer, phase-locked loop, automotive radar, VCO, injection-locked divider, dual-band, millimeter-wave.

I. INTRODUCTION

The proliferation of various millimeter-wave (MMW) frequency bands allocated by the Federal Communications Commission (FCC) has enabled new generations of short- and long-range automotive radar sensors. MMW automotive radars have mostly been implemented in fast, expensive III-V compound semiconductor technologies as monolithic microwave integrated circuits (MMICs). This is primarily because of the extremely high frequency of operation mandated by these radar transceivers. Recent advances in silicon (Si) and silicon-germanium (SiGe) technologies have made it possible to design silicon-based MMW integrated circuits [1]-[3].

Low cost requirements will necessitate multiband operation with lower component count in future generations of radar sensors. For instance, long and short-range detection can potentially be combined by integration of 24GHz and 77GHz radars on a single chip. This paper addresses the design of a dual-band frequency source for such systems.

W-band VCOs and frequency synthesizers have been reported in both SiGe [2], [4], and CMOS [5]-[6] technologies recently. Most of the reported synthesizers suffer from either high power dissipation, limited tuning range or high reference frequency. This paper presents a low-power K/W-band frequency synthesizer in a 0.18 μm SiGe BiCMOS process with 200GHz f_T/f_{max} heterojunction bipolar transistors (HBTs). All components except the loop filter are integrated on-chip. The synthesizer has been designed for integration with a dual-band automotive radar transceiver. It can potentially be used in a 94GHz heterodyne receiver by utilizing the 77GHz VCO

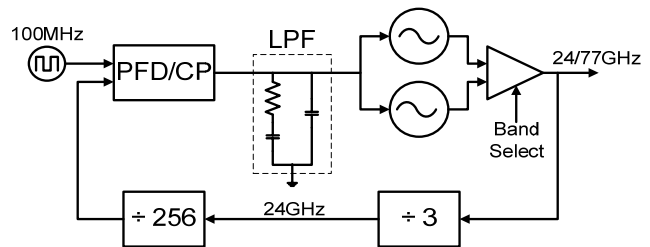


Fig. 1: Block diagram of the dual-band frequency synthesizer

output as the first local oscillator (LO) and the divide-by-6 output as the second LO.

The remainder of this paper is organized as follows: Section II discusses the synthesizer architecture and circuit design of the constituent circuits. Measurement results are presented in Section III. Finally, Section IV provides concluding remarks.

II. DESIGN OF DUAL-BAND MMW FREQUENCY SYNTHESIZER

The block diagram of the charge pump-based phase-locked frequency synthesizer is shown in Fig. 1. It consists of two LC VCOs, a divide-by-3 injection-locked frequency divider (ILFD), a divide-by-32 emitter-coupled logic (ECL) frequency divider, a divide-by-8 static CMOS frequency divider, a CMOS phase frequency detector (PFD), a CMOS charge pump (CP) and an off-chip low pass filter (LPF). In the W-band mode, the 77GHz VCO is enabled and the divide ratio is 768. The ILFD is locked to the 77GHz VCO output. In the K-band mode, the 24GHz VCO is enabled. In this mode, the ILFD is locked to the 24GHz VCO output and thus acts as a buffer, resulting in a divide ratio of 256. Although the ILFD could be used as the VCO for the K-band mode (with the 77GHz VCO disabled), the ILFD phase noise is inadequate for this purpose. This is because the ILFD in this work incorporates a tank with a low quality factor (Q) in order to achieve maximum injection-locking range. The proposed scheme allows the use of the same low phase-noise reference in both operating bands of the synthesizer. The reference frequency of the frequency synthesizer is 92-105MHz. Details of the circuit design of the synthesizer building blocks are discussed next.

A. 24GHz and 77GHz Voltage Controlled Oscillators

Fig. 2(a) shows the circuit schematic of the 77GHz VCO. It is based on a differential Colpitts topology. Microstrip transmission lines $T_{1,2}$ are used at the HBT base terminals to realize small inductance values ($\sim 25\text{pH}$) with a high Q (~ 20).

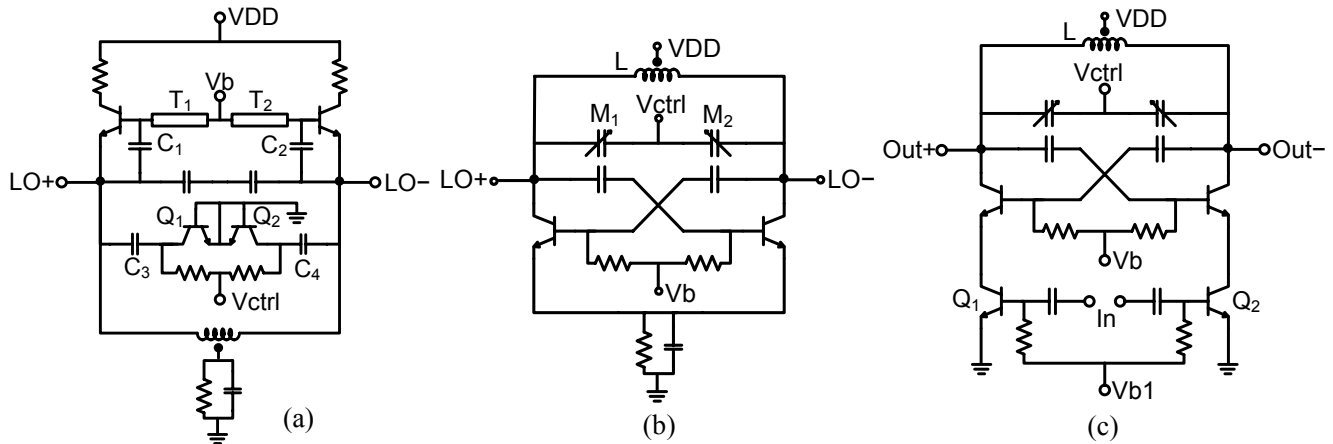


Fig. 2: Schematics of (a) 77GHz VCO, (b) 24GHz VCO, and (c) 77GHz divide-by-3 injection-locked frequency divider.

Inductive degeneration is used to improve phase noise [4] and frequency-voltage linear range. Resistive biasing is used to avoid additional noise contributions due to transistors in a conventional active tail current source. MIM capacitors $C_{1,2}$ connected between the transistor base and emitter terminals reduce the effect of voltage-variant base-to-emitter device capacitance non-linearity on VCO phase noise. HBT varactors $Q_{1,2}$ with variable base-collector junction capacitance ($Q \approx 10 @ 77\text{GHz}$) are used for frequency tuning as the Q of $0.18\mu\text{m}$ MOS varactors is inadequate at 77GHz. Differential operation is achieved by connecting two MIM capacitors $C_{3,4}$ across the emitters of the two HBTs. The VCO has been designed for a center frequency of 78GHz with a tuning range of 4GHz.

A differential cross-coupled LC oscillator topology is used for the 24GHz VCO, as shown in Fig. 2(b). The center-tapped inductor L and accumulation-mode MOS varactors $M_{1,2}$ form the VCO tank. Similar to the 77GHz VCO, resistive biasing is used to avoid phase noise degradation. The simulated tuning range of the VCO is from 24GHz to 28.5GHz.

Both VCOs are followed by two emitter-follower buffer stages, to provide sufficient isolation from the output load, and an open-collector differential amplifier stage. The open-collector outputs of the 24GHz and 77GHz differential buffer chains are tied together and then connected to the load resistors. A digital signal is used to switch between the two bands by turning on or off the NMOS tail current sources in the two differential pairs.

B. 77GHz Injection-Locked Divide-by-3 Frequency Divider

Harmonic injection-locked frequency dividers are attractive at millimeter-wave frequencies as they have low power consumption and provide flexibility in the choice of division ratio. Static frequency dividers can be used at these frequencies [2] but at the cost of higher power dissipation and higher phase noise. In this paper, a cascode HBT-based injection-locked LC oscillator, based on the work reported in [7]-[8], has been used to realize a division ratio of three. As shown in Fig. 2(c), it consists of a cross-coupled LC VCO with the tail current source replaced by a pair of input

common-emitter HBT amplifiers $Q_{1,2}$. Without an input signal, the circuit operates as a free-running oscillator at 24GHz. When a 77GHz differential input signal is applied, it modulates the free-running state of the LC tank. Due to the non-linearity of the cross-coupled pair, several intermodulation products result from the multiplication of the input signal and the tank oscillation. For a sufficiently large input signal, the output is locked to the intermodulation product at one-third of the input frequency.

ILFD circuits typically suffer from a limited locking range. In this work, the tank Q , the varactor $C_{\text{max}}/C_{\text{min}}$ ratio, and the input amplifier gain have all been optimized in order to maximize the locking range and the free-running tuning range. The tank inductance has a Q of $9 @ 25\text{GHz}$ and MOS varactors have been used to provide a tuning range from 24.5GHz to 28.3GHz. The divider power consumption is 15mW in the 77GHz mode.

In the 24GHz mode, the divider acts as a tuned buffer and locks to the VCO output frequency. Since the amplifier gain is higher at 24GHz, the current consumption can be decreased to obtain the same locking range as that in 77GHz mode. The minimum power dissipation in the 24GHz mode is 5mW.

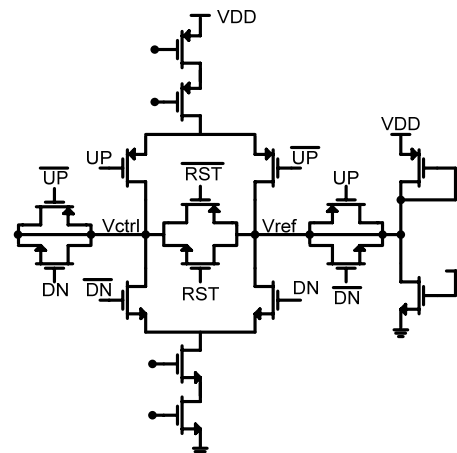


Fig. 3: Simplified schematic of the charge pump. Bias details not shown.

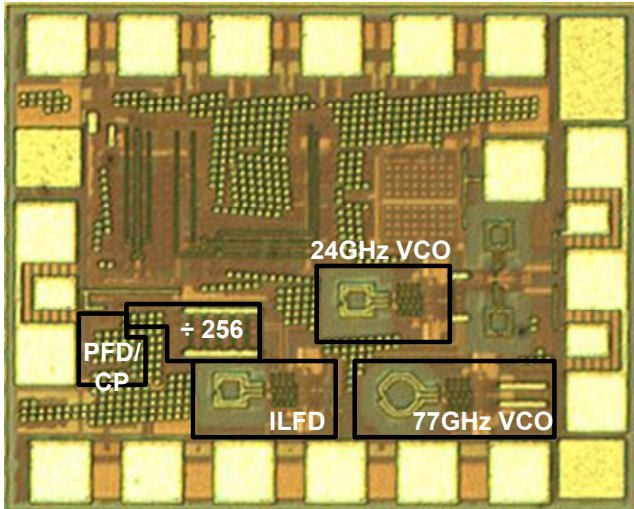


Fig. 4: Die micrograph of the dual-band frequency synthesizer. Chip size is $1 \times 0.8\text{mm}^2$.

C. Divider Chain, PFD/CP and Loop Filter

A chain of five static ECL dividers follows the ILFD and consumes only 15mW. Three static flip-flop based CMOS dividers further divide the frequency down to the reference frequency and provide a rail-to-rail signal at the input of a standard tri-state PFD. Gradual increment of the signal amplitude through the ECL divider chain, optimized for low power-consumption, efficiently eliminates the need for an ECL-to-CMOS converter prior to the CMOS divider chain.

The charge pump schematic, inspired by the topology in [9], is shown in Fig. 3. Cascode current sources reduce the effect of the VCO control voltage variation on the charge pump UP/DOWN currents until V_{ctrl} comes within $2V_{\text{dsat}}$ of the supply rails, which in turn broadens the linearity of the PLL loop. Also it reduces the UP/DOWN current mismatch. The use of a dummy branch to steer the charge-pump current for the time when V_{ctrl} is not integrating any charge, plus the charge injection and clock feed-through cancellation provided by the dummy switches, reduce the non-idealities of the charge pump circuit. The loop filter is placed off-chip to compensate for any frequency modeling errors in the MMW circuits. A Spectre-RF/Verilog-A co-simulation methodology

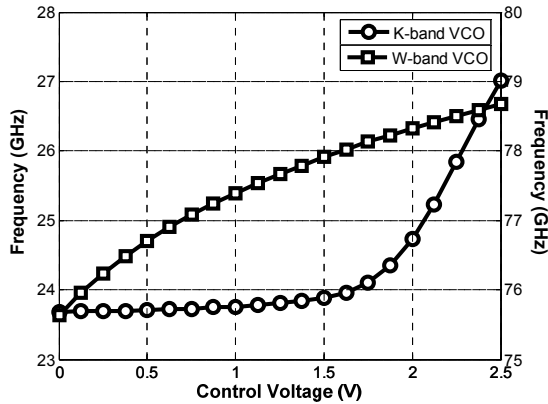


Fig. 5: Measured tuning range of the two VCOs.

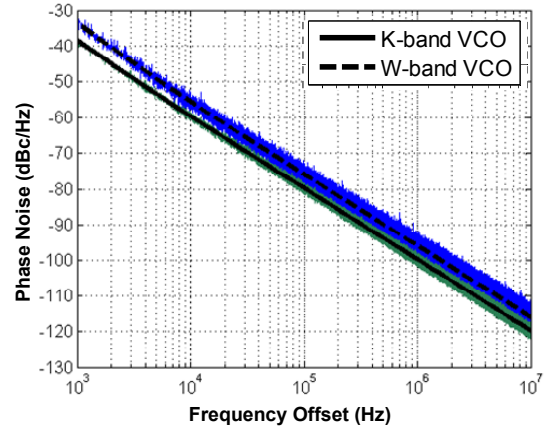


Fig. 6: Measured phase noise of the free-running VCOs.

was adopted for closed-loop simulations of the frequency synthesizer. The synthesizer has been optimized for a target loop bandwidth of 1MHz.

III. MEASUREMENT RESULTS

The dual-band frequency synthesizer was fabricated in a $0.18\mu\text{m}$ 200GHz $f_{\text{tr}}/f_{\text{max}}$ SiGe BiCMOS process with six metal layers. The $2.8\mu\text{m}$ -thick top metal was used to realize inductors and transmission lines in the VCOs and ILFD. Signal distribution between building blocks was done in the $1.6\mu\text{m}$ -thick penultimate metal to minimize coupling to the oscillator tanks. Fig. 4 depicts the micrograph of the $1 \times 0.8\text{mm}^2$ chip.

On-wafer measurements were carried out to characterize the synthesizer performance. A WR-10 waveguide-based setup was used for the 77GHz mode, including an Agilent 11970W harmonic mixer. The reference signal is provided by a 50-125MHz voltage controlled crystal oscillator. The divider chain was disabled to measure the free-running VCOs. The K-band VCO achieves a tuning range from 23.68GHz to 27GHz while the W-band VCO can be tuned from 75.6GHz to 78.6GHz, as shown in Fig. 5. The phase noise of the two VCOs is shown in Fig. 6 and is better than -95dBc/Hz at 1MHz offset from the carrier.

The output spectrum of the locked synthesizer in the two bands is shown in Fig. 7. The reference spurs at the output are 47-50dB below carrier. The synthesizer can be locked from 23.8GHz to 26.95GHz and 75.67GHz to 78.5GHz in the two bands. The output power of the synthesizer is -9.5dBm at 25.6GHz and -17.8dBm at 76.8GHz after de-embedding the losses of the measurement assembly. Fig. 8 shows the closed-loop phase noise performance of the synthesizer along with the phase noise of the reference input. The locked 24GHz VCO output shows a phase noise of -112dBc/Hz , -114dBc/Hz and -117dBc/Hz , at 100kHz, 1MHz and 10MHz offsets from the carrier, respectively. The corresponding phase noise of the locked 77GHz VCO output is -102dBc/Hz , -103.5dBc/Hz and -116dBc/Hz , respectively.

The frequency synthesizer consumes 50mW in the 24GHz mode and 75mW in the 77GHz mode. The 77GHz and 24GHz VCOs require 10mA and 4mA, respectively. The ILFD consumes a maximum of 6mA.

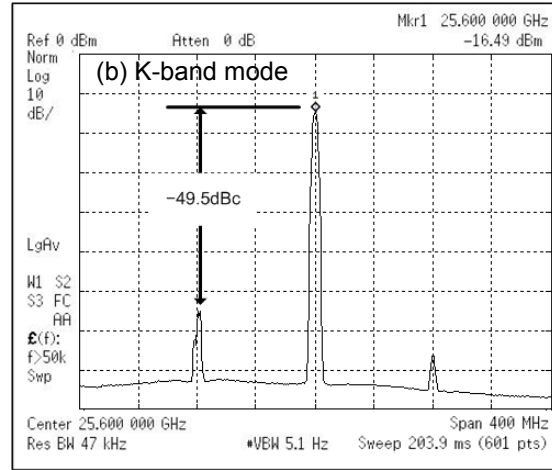
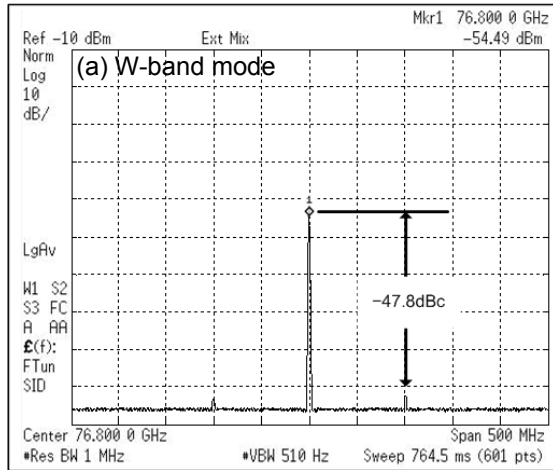


Fig. 7: Measured output spectrum of the synthesizer in (a) the W-band mode and (b) the K-band mode. Measurement setup losses have not been de-embedded.

The measured performance of the dual-band synthesizer is summarized in Table I.

IV. CONCLUSION

Design and implementation of a dual-band MMW frequency synthesizer in a 0.18 μm BiCMOS technology has been demonstrated. The highly-integrated synthesizer targets 24/77GHz automotive radars, and is also suitable for 94GHz imaging applications. Measurements of the fabricated prototype demonstrate excellent results. The locking range of the synthesizer is from 23.8GHz/75.67GHz to 26.95GHz/78.5GHz. The phase noise performance is better than -100dBc/Hz at 1MHz offset from the carrier. Use of a divide-by-3 frequency divider results in a low power consumption of 50-75mW. This work represents the first step towards the realization of fully-integrated dual-band MMW radar transceivers.

ACKNOWLEDGMENTS

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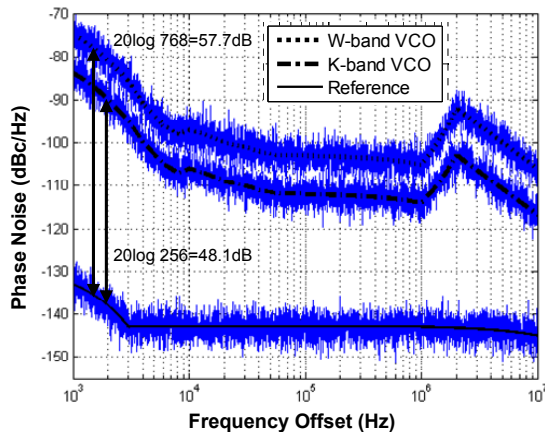


Fig. 8: Measured phase noise of the locked synthesizer output. Reference phase noise is limited by noise floor of spectrum analyzer.

TABLE I
SUMMARY OF THE MEASURED PERFORMANCE

	K-band	W-band
Locking Range	23.8-26.95GHz	75.67-78.5GHz
Phase Noise	-114dBc/Hz@1MHz	-103.5dBc/Hz@1MHz
Spurs	-49.5dBc	-47.8dBc
Output Power	-9.5dBm	-17.8dBm
Settling Time	<25 μs	<25 μs
Power Dissipation	50mW	75mW
-VCO	10mW	25mW
-ILFD	5mW	15mW
-Static Divider	15mW	15mW
-PFD/CP	5mW	5mW
Technology	0.18 μm BiCMOS	
Die Area	1x0.8mm ²	

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