

# Low-Voltage Low-Power Delta-Sigma A/D Design for Broadband Applications

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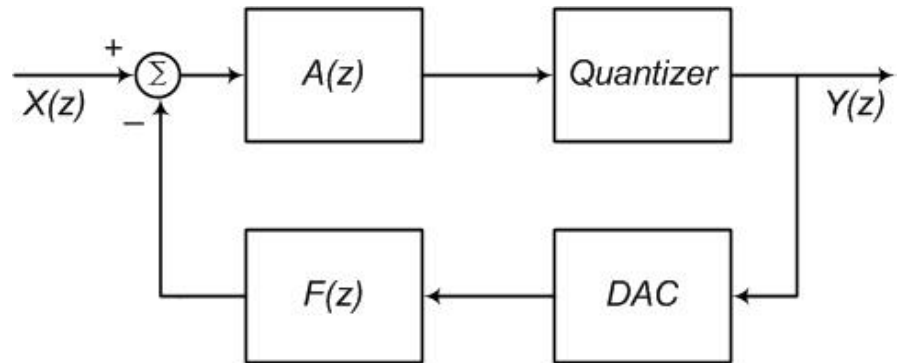
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# Introduction

- Delta-Sigma modulation is classified as a low-speed high-resolution technique for analog-to-digital conversion. Analog blocks precision requirement is traded for increased sampling rate in these kind of converters.
- Design of a 12-bit 2MHz signal bandwidth delta-sigma ADC with less than 8mW in 0.18  $\mu\text{m}$  CMOS process with 1.8V supply is presented.



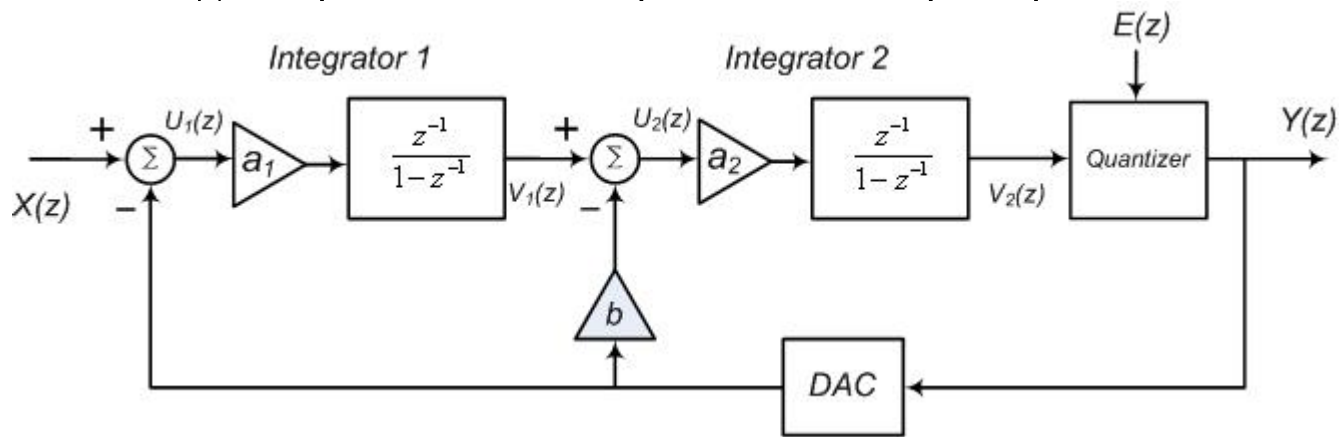
Simplified block diagram of a  $\Delta\Sigma$  ADC

# Conventional $\Delta\Sigma$ Topologies

Problems of having large signal components at the input and output of the integrators in conventional  $\Delta\Sigma$  topologies:

- At the input  $\longrightarrow$  increasing the op amps slew rate requirement
- At the output  $\longrightarrow$  limiting the stable input range  
signal dependent op amp gain variation distortion

Hence, increasing the power consumption of the op amps with low supply.



A typical conventional 2<sup>nd</sup>-order modulator.

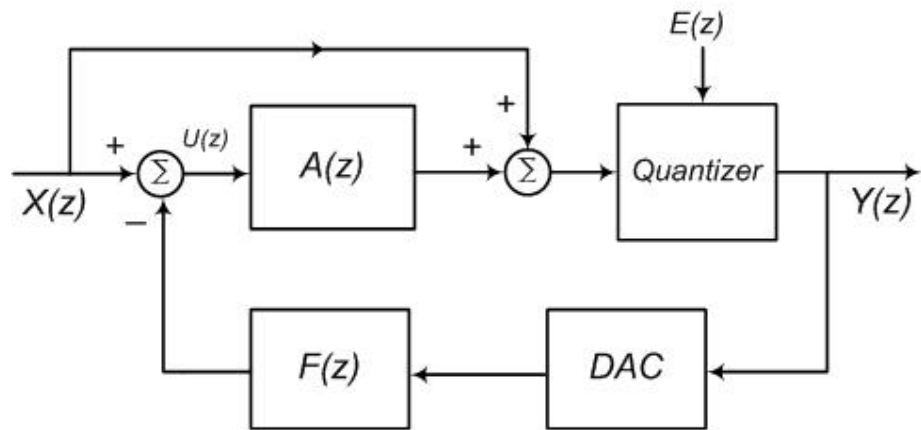
# Input Feed-forward Topology

Advantages of the input feed-forward topology:

- Reduced swing at the input and output of integrators  
    ➡ reducing the chance of slew rate  
    possibility of using single-stage op amp
- Decoupling integrators output from input signal ➡ larger stable input range
- Relaxing the DC gain and bandwidth requirements of the op amps

Main disadvantage is the timing issue of the loop created by adding the input feed-forward path.

Hence, totally the benefits outweigh.



Block diagram of input feed-forward topology

# Fully Digital Input Feed-forward Topology<sup>1</sup>

Retains the advantages of the input feed-forward topology

✦ improves the SQNR and eliminates of the analog adder

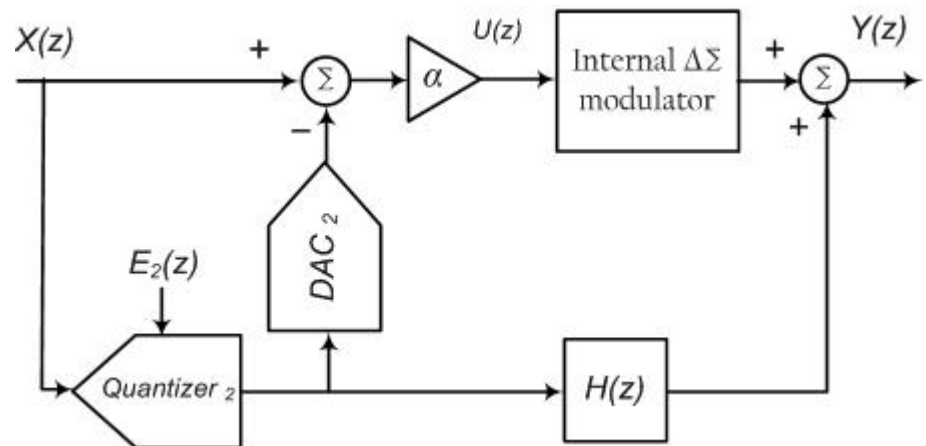
Requires an extra quantizer and digital adders

0-L MASH topology is basically an special case of the FDFE topology

Assuming  $H = \alpha \cdot STF_{\Delta\Sigma}$

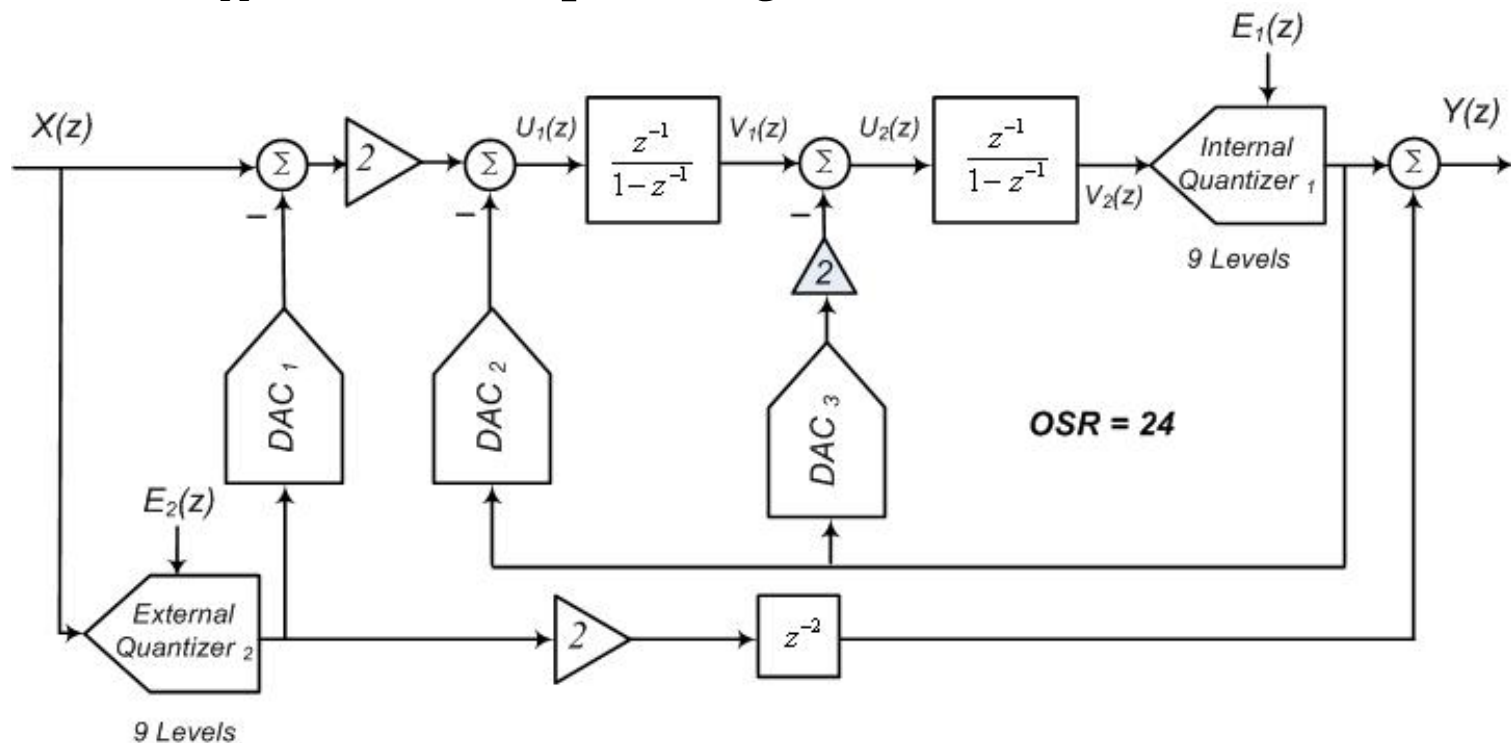
Output equation:

$$Y = (\alpha \cdot STF_{\Delta\Sigma}) \cdot X + NTF_{\Delta\Sigma} \cdot E_1$$



# 0-2 MASH FDFFF Topology

- 96MHz sampling frequency (OSR = 24)
- 12-bit resolution (SNDR = 74dB)
- Two 9-level quantizers
- 0dBFS =  $2V_{PP}$  differential input swing



# High-Level Design

- Integrators coefficients were chosen by dynamic range scaling  
(only 6 comparators of the internal quantizer are required)
- Folded cascode op amp with  $1.6V_{PP}$  differential output swing was assumed.
- Designed for worst case simulation results of three different input freq.
- Ideal modulator 81.5dB SQNR at 0dBFS
- Unit capacitor size = 32fF gives  $SNR_{thermal} = 77.9dB$

$$P_{thermal} = \left(1 + \frac{C_{DAC1\ total}}{C_{S1}}\right) \cdot \frac{4KT}{C_{S1}} \cdot \frac{1}{OSR} + \left(1 + \frac{C_{DAC2\ total}}{C_{S2}}\right) \cdot \frac{4KT}{C_{S2}} \cdot \frac{\pi^2}{3\ OSR^3} \cdot \frac{1}{\alpha^2}$$

- 2<sup>nd</sup>-integrator capacitors are determined by matching considerations.

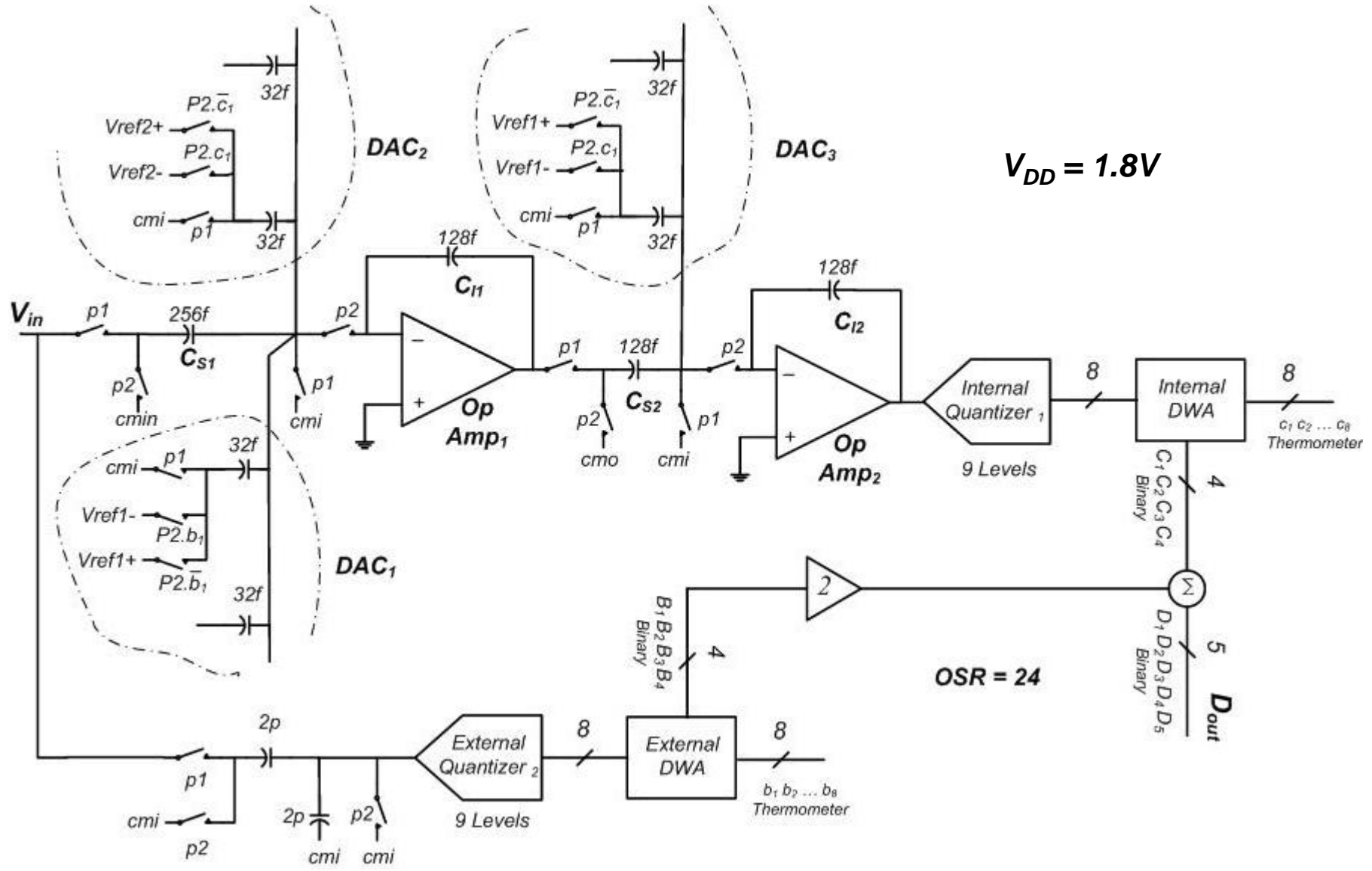
# Op Amp Requirements

- Op amps were designed for worst case simulation results of three different input freq.
- Op amps were separately optimized.

Specification	1st Op Amp	2nd Op Amp
Open Loop DC Gain	83dB	72dB
Closed Loop -3dB BW	200MHz	115MHz
Open Loop Unity Gain Freq	1.4GHz	460MHz
SlewRate	370V/ $\mu$ s	225V/ $\mu$ s
Feedback Factor	$\frac{1}{7}$	$\frac{1}{4}$

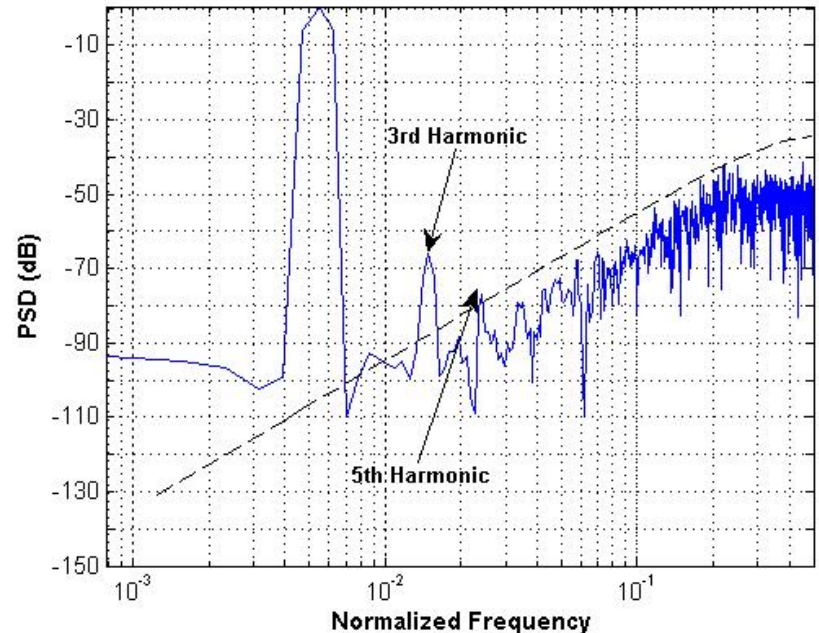
- Op amps are bandwidth-limited.
- Modulator with the non-ideal integrators achieved more than 78dB SQNR for 0dBFS input.

# Switched-Capacitor Circuit



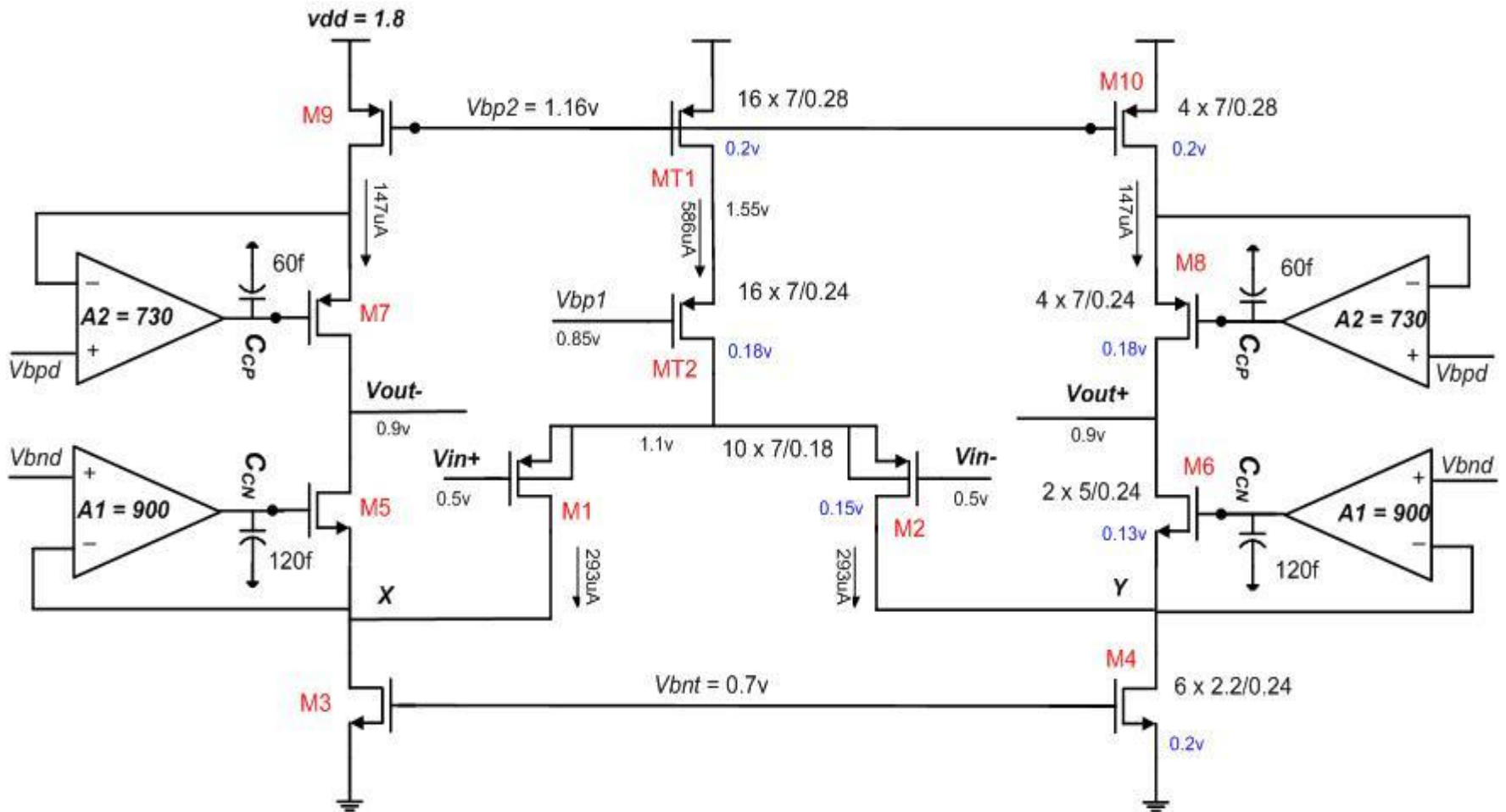
# Telescopic Op Amp Problem

- Using an optimized size NMOS for the switch near the first op amp input terminal can reduce the SNDR to 69dB at 0dBFS in the slow-slow 80C corner.
- Different kinds of switching were investigated. 85dB SNDR was achieved for typical corner, but due to the midrail input common mode voltage of the telescopic op amp the slow-slow 80C corner results was not good enough.



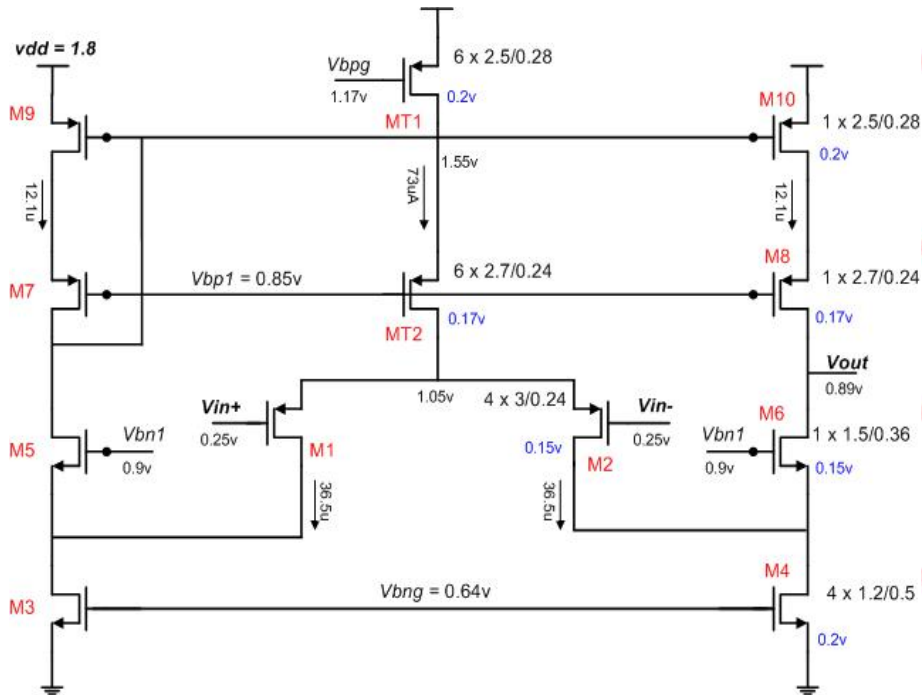
Sample output spectrum with telescopic op amps

# Folded Cascode Op Amp

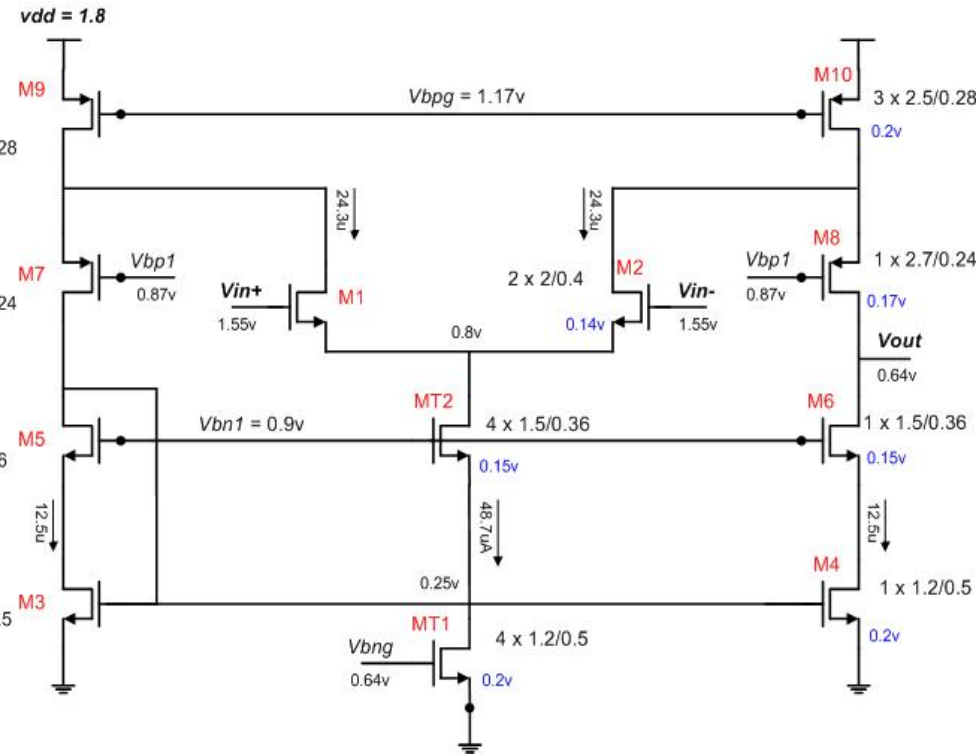


$V_{eff}$  voltages are indicated in blue color.

# Gain Boosting Amplifiers



NMOS side amplifier



PMOS side amplifier

# Op Amp Simulation Results

Op amps were designed to meet the requirements in slow-slow 80C, fast-fast 0C, and typical 80C corners.

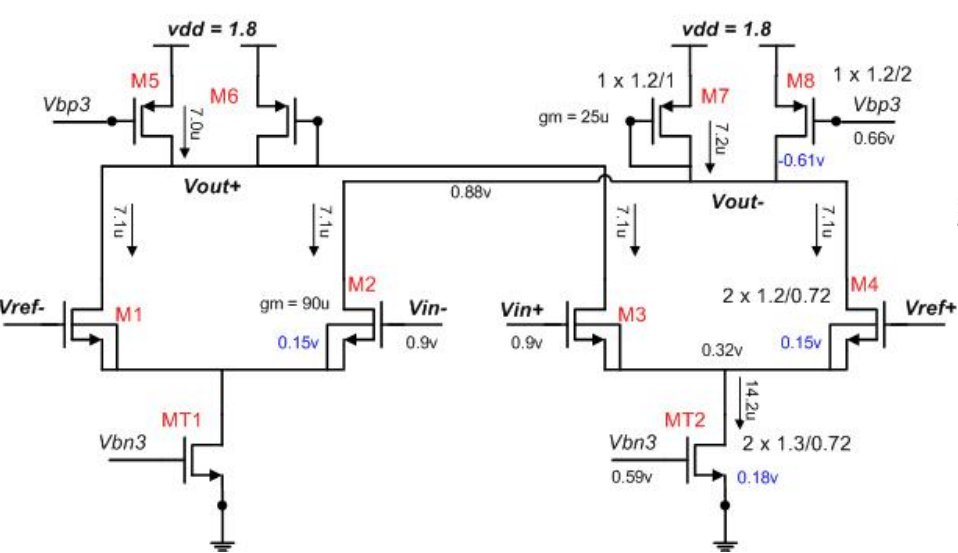
Specification	1st Op Amp	2nd Op Amp
Open Loop DC Gain	108dB	107dB
Loop DC Gain	90dB	94dB
Closed Loop -3dB BW	294MHz	195MHz
Open Loop Unity Gain Freq	1.63GHz	550MHz
Loop Phase Margin	74 deg	78 deg
0.1% Settling Time	2.2ns	4.4ns
Slew Rate	1.4V/ns	460V/ $\mu$ s
Offset (sigma)	3.3mV	6.8mV
Total Power Consumption	2.2mW	860 $\mu$ W

Typical 80C results

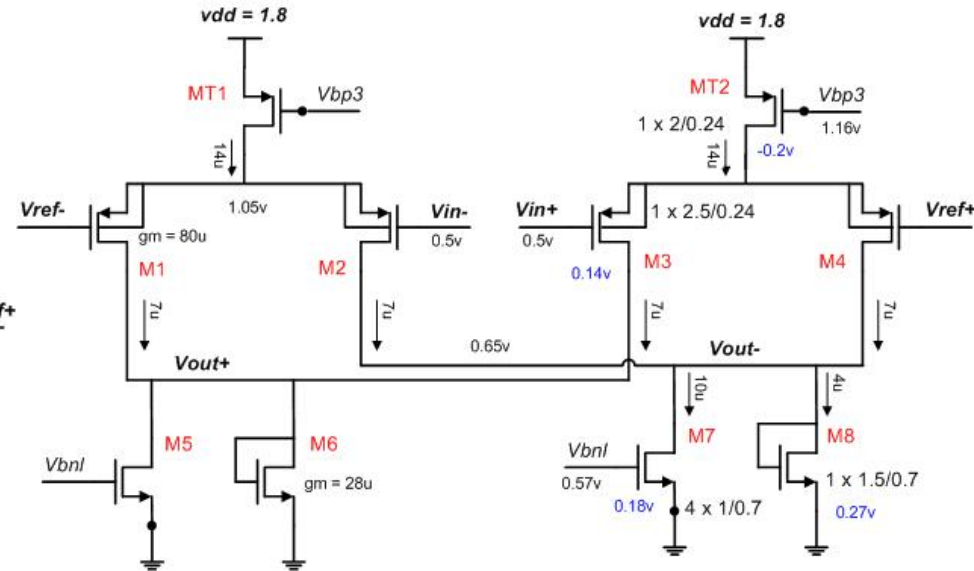


# Quantizers

- Both 9-level quantizers are realized as flash ADCs.
- Comparators are implemented by cascading preamps and regenerative latches.



Internal quantizer preamps



External quantizer preamps

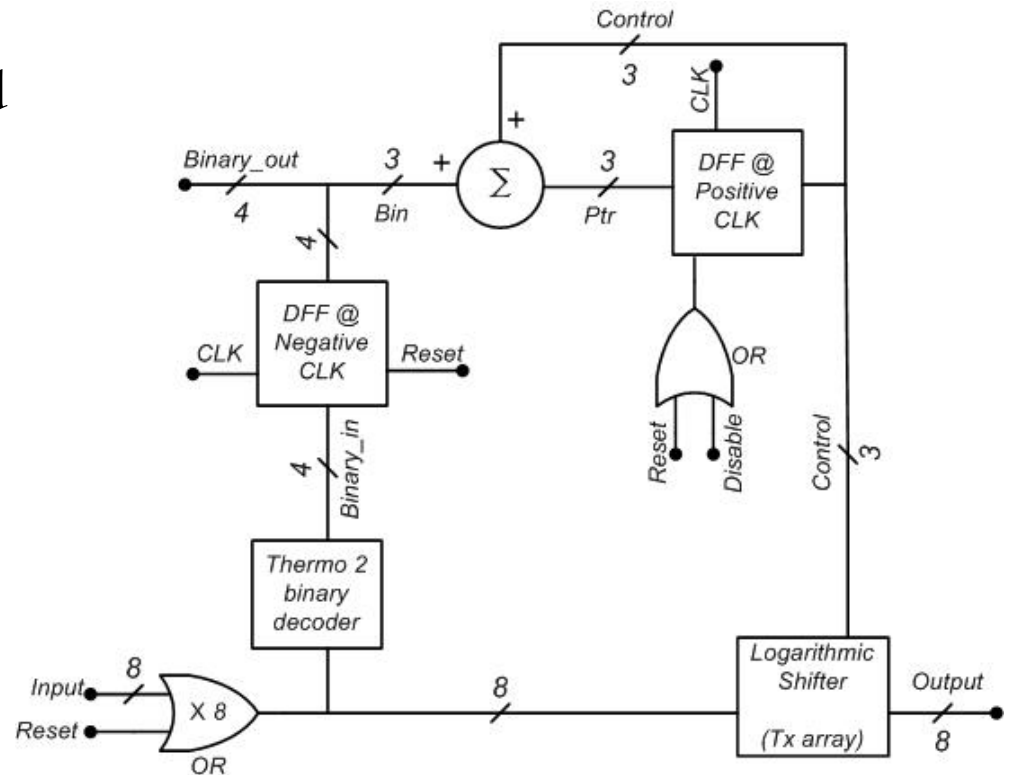


# Data Weighted Averaging

DWA was chosen for DAC linearization.

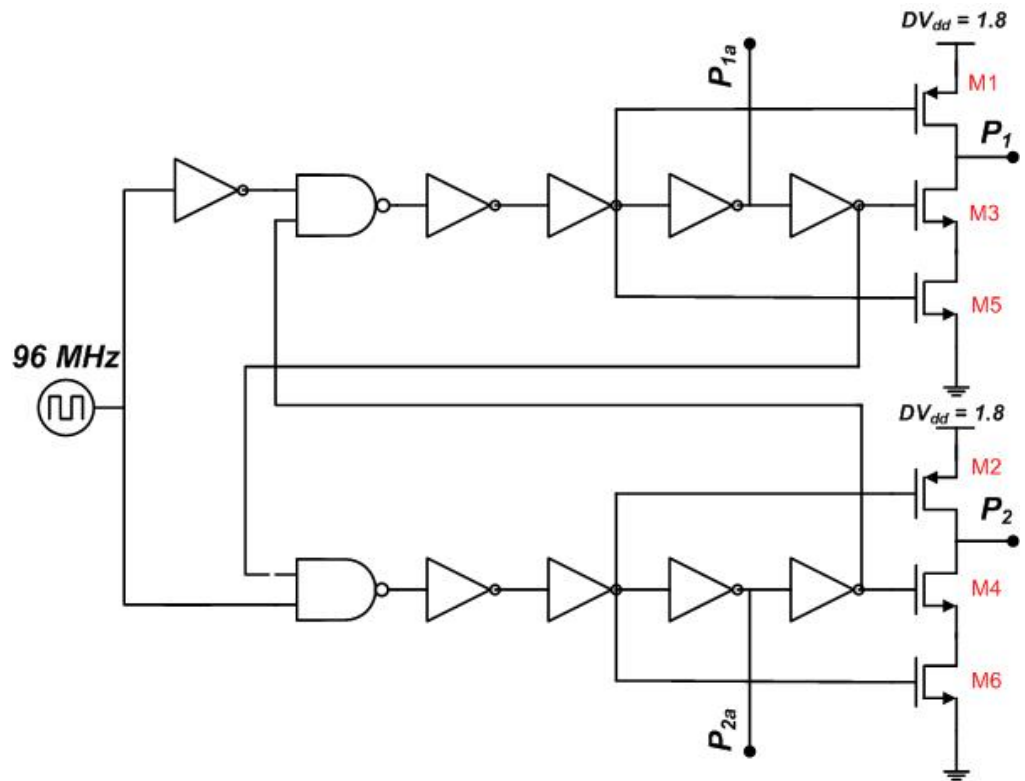
The same DWA circuit was used for both of the quantizers.

The logarithmic shifter was implemented as an array of transmission gates, as it was faster than an array of NMOS transistors.



# Clock Generation

- A 96MHz square wave input is applied to the chip.
  - Non-advanced phases durations are 4.5ns (typical 80C).
  - Advanced phases durations are 4.2ns (typical 80C).
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- Rising edge of the advanced and non-advanced phases are matched to within 50ps for different corners.



# Power Consumption Summary

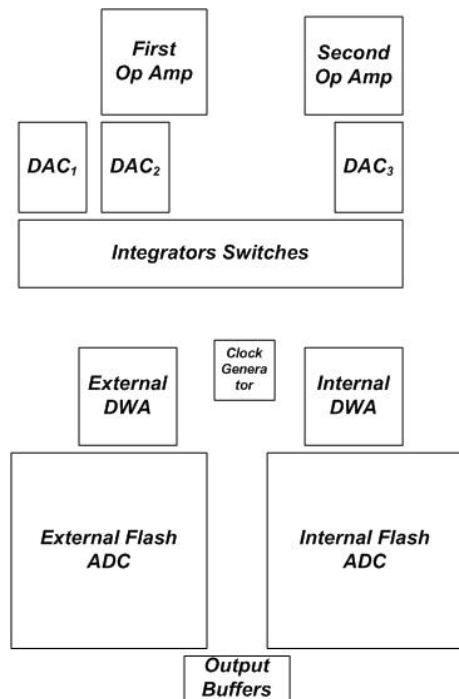
Block	Current ( $\mu\text{A}$ )	Power ( $\mu\text{W}$ )
Total Analog	2.32 mA	4.2 mW
1st Op Amp	1.22 mA	2.2 mW
2nd Op Amp	480	860
Op Amps Bias	130	240
Total Bias	240	440
Internal Flash Premaps	150	270
External Flash Premaps	220	400
Total Digital	0.87 mA	1.6 mW
Total Flash Latches	60	110
DWAs	200	370
Clocks	490	880
Other Digital	120	230
Total	3.19mA	6.4 mW

Schematic-level power consumption summary (typical 80C)

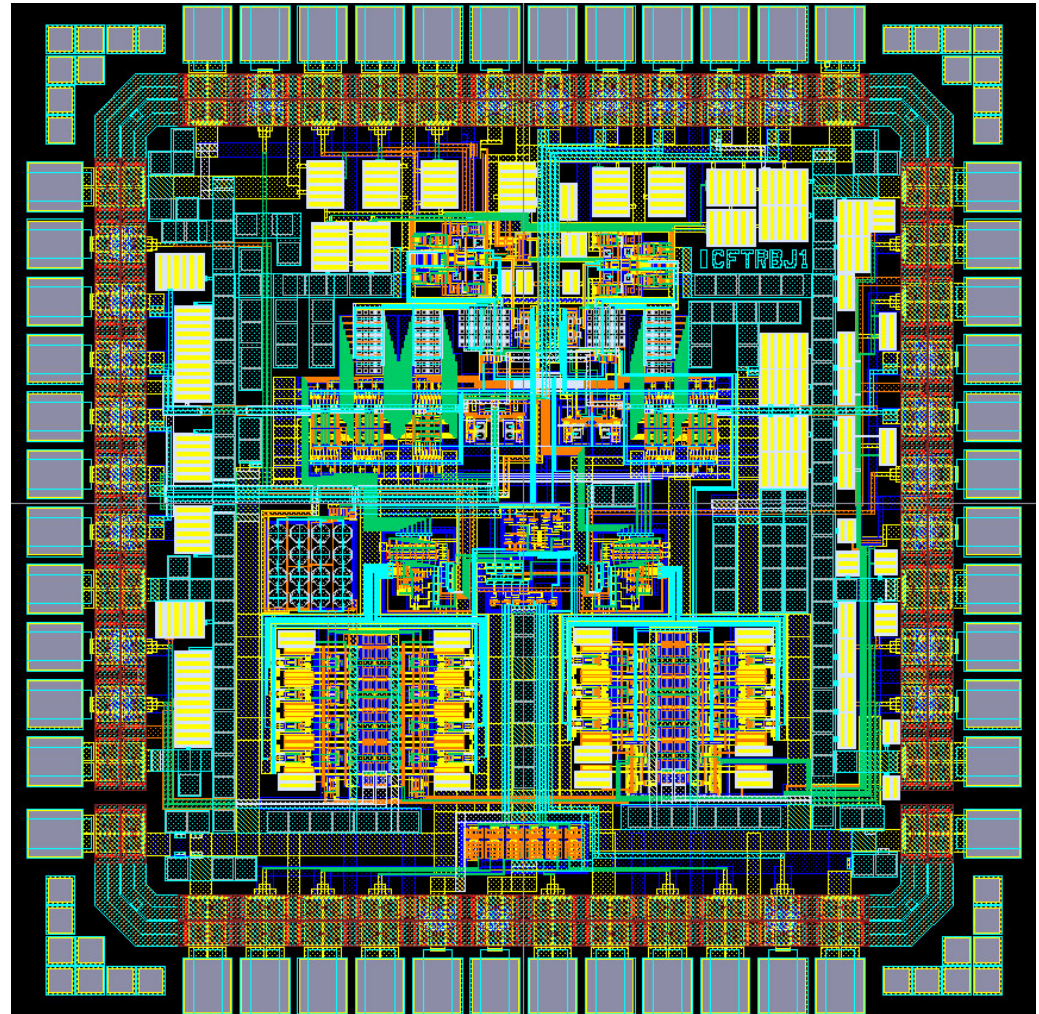
# Layout

Core area =  $750\mu\text{m} \times 750\mu\text{m}$   
Total area =  $1.4\text{mm} \times 1.4\text{mm}$

5 binary data output pins  
1 clock output pins

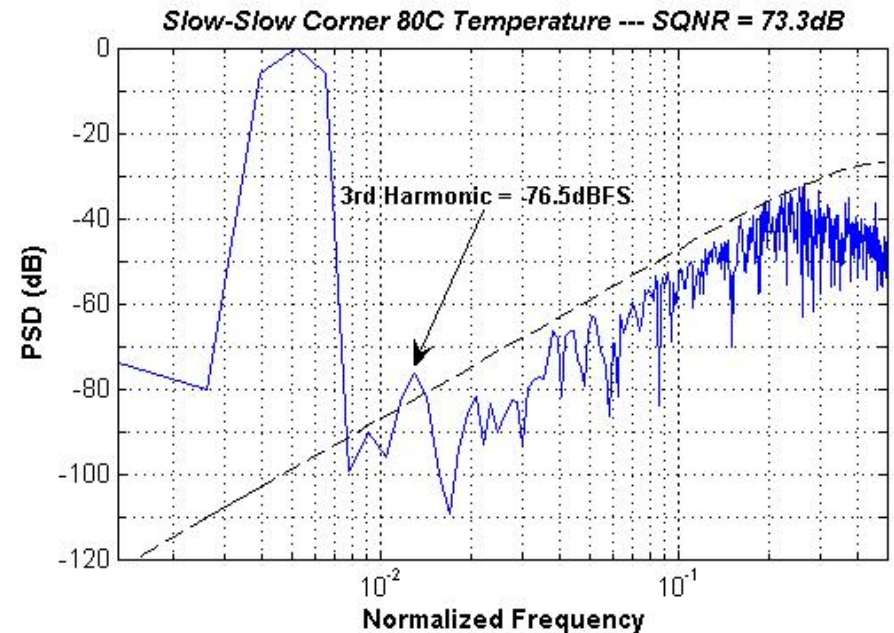
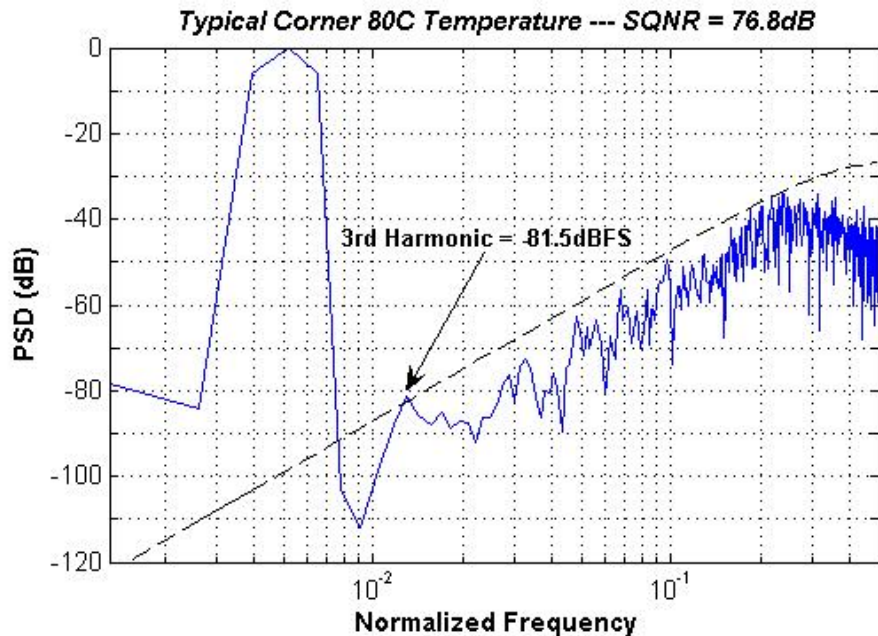


Floor plan



Chip complete layout

# Post Layout Simulation Results



Digital power has increased by 80%.

Block	Current	Power
Total Analog	2.38 mA	4.3 mW
Total Digital	1.61 mA	2.9 mW
Total	3.99mA	7.2 mW

# Conclusion

- A 12-bit 2MHz signal BW delta-sigma ADC with 7.2mW total analog and digital power consumption was designed and presented.
- The complete ADC except the voltage references and the decimation filter was integrated on-chip using a 0.18 $\mu$ m CMOS process. Both analog and digital circuitry use only 1.8V supplies.
- Post layout simulations for different process and temperature corners showed promising results. According to post layout simulation results, the power efficiency of this work is comparable to previously published work.
- A new efficient low-voltage low-power broadband  $\Delta\Sigma$  topology was investigated.